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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,123	12/29/2000	Calvin Guey	JCLA6706	8730

7590 11/19/2003

J.C. PATENTS INC.
4 VENTURE
SUITE 250
IRVINE, CA 92618

EXAMINER	
GOLE, AMOL V	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

Office Action Summary	Application No.	Applicant(s)	
	09/752,123	GUEY ET AL.	
	Examiner	Art Unit	
	Amol V. Gole	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/29/00;6/8/01;9/14/01;2/24/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Receipt is acknowledged of the following papers:

1) Priority papers (6/8/01)

2) Change of address (9/14/01)

3) Change of address (2/24/01)

These papers have been placed of record in the file.

2. Claims 1-12 have been examined.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Oath/Declaration

4. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

The title of the invention referred to in the declaration is not the same as the title of the application.

Specification

5. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

6. The abstract is objected to because it does not include the technical disclosure of the improvement over an old method. Please make the necessary corrections.

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

8. The following title is suggested: APPARATUS AND METHOD FOR COPROCESSOR DATA ACCESS CONTROL AND INSTRUCTION FORMAT THEREWITH.

9. The disclosure is objected to because of the following informalities:

1) The disclosure does not refer to and explain the label "CS" in Fig. 1.

2) The specification mentions that each coprocessor will access or retrieve a fixed-length words from the memory according to the value in the coprocessor number field **and/or** coprocessor register field (pg. 6, lines 8-10). However, what decides whether the number field is used or the register field is used or both are used as the indicating field is unclear. Furthermore, how both the fields can be used together to indicate the number of data words to be accessed is also unclear.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. The claim recites the limitation that the number of word data depends on the value in the coprocessor number field **and/or** the value in the coprocessor register field. This limitation is unclear because of the use of "and/or". It is not clear when to use "and" and when to use "or". Moreover, how the number of word data to be accessed can depend on both the coprocessor number field **and** the coprocessor register field is not clear. Henceforth the claim will be interpreted differently for "and" and for "or".

Claim Rejections - 35 USC § 101

13. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

14. Claims 9-12 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. An instruction format not claimed as embodied in a computer readable media is descriptive material *per se* and is not statutory because it is not capable of causing functional change in the computer. Alternatively an instruction format can also be interpreted as a nonfunctional descriptive material as it is simply a mere arrangement of data that is stored so as to be read or outputted by a computer without creating any functional interrelationship, either as part of the stored data or as part of the computing processes preformed by the computer, which alone does not impart functionality either to the data as so structured, or to the computer.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1, 3, 5, 7, 9 and 11 rejected under 35 U.S.C. 102(b) as being anticipated by York et al. (US006002881A).

17. In regard to Claim 1:

18. York et al. disclose an apparatus for coprocessor data access control (col. 1, line 65), comprising

1) a central processing unit, for executing central processing unit instructions to perform data processing, wherein the central processing unit instructions includes a plurality of coprocessor memory access instructions (col. 1, lines 66-67; col. 2, lines 1-2);

2) a memory unit, coupled to the central processing unit, for storing data words (col. 2, lines 3-4) ; and

3) a coprocessor, coupled to the central processing unit and the memory unit, for accessing and processing the data words stored in the memory unit by one of addressing modes under control of the coprocessor memory access instructions executed by the central processing unit (col. 2, lines 5-10), wherein

the coprocessor memory access instruction having an indicating field (portion of addressing mode information, col. 2, line 15), and data words are accessed to or from the memory unit by the coprocessor according to the value of the indicating field (to control how many data words are transferred between said memory, col. 2, lines 28-29).

Although, York et al. mention that data words are accessed to or from the memory unit by the coprocessor, they are silent on how many data words are accessed. However, it would be deemed inherent to the York et al. apparatus to access N data words where N is a value greater than or equal to 1. The objective of the apparatus of accessing data words would not be met if no data words accessed, i.e. N is equal to 0. Hence, if N data words are transferred, N must be a value greater than or equal to 1.

19. In regard to Claim 3:

20. York et al. disclose that the indicating field (portion of addressing mode information, col. 2, line 15) of the coprocessor memory access instruction includes or is a coprocessor register field (register numbers, col. 2, lines 19-20; col. 63,64, lines 10-20, bits 12-15/bits 0-7), for storing information about specific registers to be used in the data processing.

21. In regard to claim 5, interpreting the "and/or" limitation as "and":

22. York et al. teaches of a coprocessor data access control method (col. 4, line 5), comprising the steps of:

1) providing an instruction (col. 4, lines 19-20) having an indicating field (portion of addressing mode information, col. 4, line 23); and

2) accessing data words to or from a memory unit by a specified coprocessor according to the value in the coprocessor indicating field (col. 4, lines 23-28), and access of the word data depends on the value in the coprocessor number field (as a destination or source field, col. 63,64, lines 10-20, bits 8-11) **and** in the coprocessor register field (register numbers, col. 2, line 20; col. 63,64, lines 10-20, bits 12-15/bits 0-7).

Although, York et al. mention that data words are accessed to or from the memory unit by the coprocessor, they are silent on how many data words are accessed. However, it would be deemed inherent to the York et al. apparatus to access N data words where N is a value greater than or equal to 1. The objective of the apparatus of accessing data words would not be met if no data words accessed, i.e. N is equal to 0. Hence, if N data words are transferred, N must be a value greater than or equal to 1.

23. In regard to Claim 7:

24. York et al. disclose that the indicating field (portion of addressing mode information, col. 2, line 15) of the coprocessor memory access instruction includes or is a coprocessor register field (register numbers, col. 2, lines 19-20; col. 63,64, lines 10-20, bits 12-15/bits 0-7), for storing information about specific registers to be used in the data processing.

25. In regard to Claim 9:

26. York et al. disclose an instruction format (col. 5 & 6, lines 1-7) for a coprocessor data access control, wherein the instruction format includes an indicating field (col. 63,64, lines 10-20, bits 12-15/bits 0-7), and a particular coprocessor to be used (bits 8-11) and the number of data words to be accessed to or from the memory unit is determined by the value of in the indicating field (register numbers, col. 2, lines 19-20).

27. In regard to Claim 11:

28. York et al. disclose that the indicating field (portion of addressing mode information, col. 2, line 15) of the coprocessor memory access instruction includes or is a coprocessor register field (register numbers, col. 2, lines 19-20; col. 63,64, lines 10-20, bits 12-15/bits 0-7), for storing information about specific registers to be used in the data processing.

Claim Rejections - 35 USC § 103

29. Claims 2, 4, 5, 6, 7, 8, 10, and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over York et al (US006002881A).

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. In regard to Claims 2 and 4:

32. York et al. teach an indicating field (bit fields, col. 2, line 19) within the coprocessor memory access instruction (col. 63,64, lines 10-20). The instruction includes a coprocessor number field (bits 8-11) and a register field (bits 12-15/bits 0-7).

33. York et al. does not explicitly mention that the indicating field includes the coprocessor number field.

34. However York et al. does teach that the bit fields (that may include register numbers [register field] and immediate constants) that are used by the central processing unit to control which of a plurality of addressing modes is used, may also be used to specify (possibly in combination with other factors, such as other fields in the instruction or values written in control registers) to the coprocessor the number of data words to be transferred (col. 2, lines 19-26). Also, York et al. teaches that by overlapping the use of the same bit space within those coprocessor memory access instructions frees up bit space for other uses (col. 2, lines 32-35) and leads to improvements in code density and efficiency (col. 2, lines 36-42).

35. One of ordinary skill in the art at the time of the invention would have easily recognized from the teachings of York et al. that the coprocessor number field could also very well be included in the indicating field to indicate the number of data words to be accessed and further reap the benefits of freeing up bit space for other uses and better code density and efficiency. Also, as York et al. teach that the bit fields may be used in combination of other fields in the instruction to specify to the coprocessor the

number of data words to be transferred, the indicating field could include both the coprocessor number field and register field.

36. Hence, it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention, to include the coprocessor number field or both the coprocessor number field and register field in the indicating field of the coprocessor memory access instruction as taught by York et al. in order to free up bit space and improve code density and efficiency.

37. In regard to Claim 5, interpreting the "and/or" limitation as "or":

38. York et al. teaches of a coprocessor data access control method (col. 4, line 5), comprising the steps of:

1) providing an instruction (col. 4, lines 19-20) having an indicating field (portion of addressing mode information, col. 4, line 23); and

2) accessing data words to or from a memory unit by a specified coprocessor according to the value in the coprocessor indicating field (col. 4, lines 23-28), and number of word data depends on the value in the coprocessor register field (register numbers, col. 2, line 20; col. 63,64, lines 10-20, bits 12-15/bits 0-7).

39. York et al. does not teach of accessing N data words, wherein N is a value greater than or equal to 1. Also York et al. do not explicitly mention that the number of word data (or N), depends on the value in the coprocessor number field (col. 63,64, lines 10-20, bits 8-11).

40. However York et al. does teach that the bit fields (that may include register numbers and immediate constants) that are used by the central processing unit to control which of a plurality of addressing modes is used, may also be used to specify (possibly in combination with other factors, such as other fields in the instruction or values written in control registers) to the coprocessor the number of data words to be transferred (col. 2, lines 19-26). Alternatively this means that the number of data words to be transferred can depend on bit fields from the coprocessor memory access instructions.

41. One of ordinary skill in the art at the time of the invention would have easily recognized from the teachings of York et al. that the number of data words can depend on the coprocessor number field.

42. Also, it would be deemed inherent to the York et al. apparatus to access N data words wherein N is a value greater than or equal to 1. The objective of the apparatus of accessing data words would not be met if no data words accessed, i.e. N is equal to 0. Hence, if N data words are transferred, N must be a value greater than or equal to 1.

43. Hence it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention that the number of word data accessed in the York et al. method can depend on the value in the coprocessor number field and/or the value in the coprocessor register field.

44. In regard to Claims 6 and 8:

45. York et al. teach an indicating field (bit fields, col. 2, line 19) within the coprocessor memory access instruction (col. 63,64, lines 10-20). The instruction includes a coprocessor number field (bits 8-11) and a register field (bits 12-15/bits 0-7).

46. York et al. does not explicitly mention that the indicating field includes the coprocessor number field.

47. However York et al. does teach that the bit fields (that may include register numbers [register field] and immediate constants) that are used by the central processing unit to control which of a plurality of addressing modes is used, may also be used to specify (possibly in combination with other factors, such as other fields in the instruction or values written in control registers) to the coprocessor the number of data words to be transferred (col. 2, lines 19-26). Also, York et al. teaches that by overlapping the use of the same bit space within those coprocessor memory access instructions frees up bit space for other uses (col. 2, lines 32-35) and leads to improvements in code density and efficiency (col. 2, lines 36-42).

48. One of ordinary skill in the art at the time of the invention would have easily recognized from the teachings of York et al. that the coprocessor number field could also very well be included in or used as the indicating field to indicate the number of data words to be accessed (e.g. by setting the coprocessor number equal to the amount of data words it accesses) and further reap the benefits of freeing up bit space for other uses and better code density and efficiency. Also, as York et al. teach that the bit fields may be used in combination of other fields in the instruction to specify to the

coprocessor the number of data words to be transferred, the indicating field could include both the coprocessor number field and register field.

49. Hence, it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention, to use the coprocessor number field or both the coprocessor number field and register field in the indicating field as taught by York et al. in order to free up bit space and improve code density and efficiency.

50. In regard to Claim 7:

51. York et al. disclose that the indicating field (portion of addressing mode information, col. 2, line 15) of the coprocessor memory access instruction includes or is a coprocessor register field (register numbers, col. 2, lines 19-20; col. 63,64, lines 10-20, bits 12-15/bits 0-7), for storing information about specific registers to be used in the data processing.

52. In regard to Claims 10 and 12:

53. York et al. teach an indicating field (bit fields, col. 2, line 19) within the coprocessor memory access instruction (col. 63, 64, lines 10-20). The instruction includes a coprocessor number field (bits 8-11) and a register field (bits 12-15/bits 0-7).

54. York et al. does not explicitly mention that the indicating field includes the coprocessor number field.

55. However York et al. does teach that the bit fields (that may include register numbers [register field] and immediate constants) that are used by the central processing unit to control which of a plurality of addressing modes is used, may also be used to specify (possibly in combination with other factors, such as other fields in the instruction or values written in control registers) to the coprocessor the number of data words to be transferred (col. 2, lines 19-26). Also, York et al. teaches that by overlapping the use of the same bit space within those coprocessor memory access instructions frees up bit space for other uses (col. 2, lines 32-35) and leads to improvements in code density and efficiency (col. 2, lines 36-42).

56. One of ordinary skill in the art at the time of the invention would have easily recognized from the teachings of York et al. that the coprocessor number field could also very well be included in or used as the indicating field to indicate the number of data words to be accessed (e.g. by setting the coprocessor number equal to the amount of data words it accesses) and further reap the benefits of freeing up bit space for other uses and better code density and efficiency. Also, as York et al. teach that the bit fields may be used in combination of other fields in the instruction to specify to the coprocessor the the number of data words to be transferred, the indicating field could include both the coprocessor number field and register field.

57. Hence, it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention, to use the coprocessor number field or both the coprocessor number field and register field as the indicating field as taught by York et al. in order to free up bit space and improve code density and efficiency.

Conclusion

58. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty, which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections. See 37 CFR § 1.111.

a. Hashimoto et al. (US005193159A) disclose a master processor and coprocessor system wherein they monitor the number of data transfers or the end of the sequence of data transfer independently so that the coprocessor does not need to receive a command from the master for each data transfer and the coprocessor does not need to indicate the end of transfer to the master hence improving the efficiency of data transfer.

b. Zolnowsky et al. (US004729094) disclose a processor to coprocessor interface, which relies wholly on standard bus cycles. Also the processor on receiving a coprocessor instruction forwards it to the specified coprocessor and remains unconcerned about the specific content of it. In col. 19, lines 23-27, they mention that a length field indicates the number of bytes transferred. If the length field is zero a protocol violation is made.

59. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amol V. Gole whose telephone number is 703-305-8888. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

AVG

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